AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A channel for electrically connecting a source and a drain of a field effect transistor (FET) comprising:

a channel core coupled to a substrate and defining a top surface spaced from the substrate and opposed sidewall surfaces between the substrate and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure;

a channel envelope in contact with the opposed sidewall surfaces and the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; ~~and~~

a gate oxide disposed about a surface of the channel envelope that is opposite the channel core.

2. (Original) The channel of claim 1 further comprising a gate coupled through the gate oxide to at least two surfaces defined by the channel envelope.

3. (Original) The channel of claim 1 wherein at least one of the sidewall surfaces defines a height h_c and the top surface defines a width w_c, and wherein $h_c \geq 3w_c$.

4. (Original) The channel of claim 1 wherein the channel is a component of an FET and the FET is a component of a SRAM, and at least one of the sidewall surfaces defines a height h_c that is selected to increase stability of the SRAM.

5. (Original) The channel of claim 1 wherein the top surface defines a width w that is selected to maximize one of stretching and of compressing the lattice structure of one of the first and the second semiconductor material.

6. (Original) The channel of claim 1 wherein the second semiconductor material substantially covers the two sidewall surfaces and the top surface.

7. (Original) The channel of claim 1 wherein one of the first and second semiconductor materials comprises silicon and germanium.

8. (Currently Amended) In a channel for a field effect ~~transmitter~~ transistor, the improvement comprising:

a channel core defining at least a top and at least one adjoining side surface;

a channel envelope in contact with the top surface and the at least one side surface;

a gate oxide disposed on at least two surfaces of the channel envelope, said surfaces of the channel envelope being opposed to the top surface and the at least one side surface,

wherein the channel core comprises a first semiconductor material and the channel envelope comprises a second semiconductor material, and at least one of the first and second semiconductor materials exhibits one of a stretched and a compressed lattice structure.

9. (Withdrawn) A method for making a FET channel comprising:

providing a substrate and a first semiconductor material overlying the substrate;

defining a first channel core from the first semiconductor material, wherein the channel core defines a top surface spaced from the substrate and opposed first and second sidewalls between the substrate and the top surface;

disposing a layer of second semiconductor material to contact at least two of the top surface, the first sidewall and the second sidewall; and

disposing a gate oxide on at least two exterior surfaces of the channel envelope that are opposed to the at least tow of the top surface, the first sidewall, and the second sidewall.

10. (Withdrawn) The method of claim 9 wherein the first semiconductor material comprises one of Si or Si_xGe_{1-x} and the second semiconductor material comprises the other of Si or Si_xGe_{1-x}.

11. (Withdrawn) The method of claim 9 wherein disposing a layer of second semiconductor material comprises masking and etching.

12. (Withdrawn) The method of claim 11 wherein defining a first channel core comprises defining a first and a second channel core spaced from one another, and disposing a layer of second semiconductor material comprises disposing said layer on the first channel core but not the second channel core.

13. (Withdrawn) The method of claim 9 wherein disposing a layer of second semiconductor material comprises disposing a carrier wafer with the layer of second semiconductor material over the first channel core, separating at least a portion of said layer from said carrier wafer, and removing said carrier wafer.

14. (Withdrawn) A method of forming a PFET channel comprising:

providing a substrate and a layer of first semiconductor material overlying the substrate;

defining a trench in said first semiconductor layer that divides said layer into a first section and a second section;

removing a portion of the second section so that a remaining layer of first semiconductor material has a thickness less than a depth of the trench, and a portion of the trench is exposed;

disposing a layer of second semiconductor material over the remaining layer and adjacent to the trench.

15. (Withdrawn) The method of claim 14 wherein the trench is filled prior to removing a portion of the second section.

16. (Withdrawn) The method of claim 14 wherein the remaining layer has a thickness less than about 15 nm.

17. (Withdrawn) The method of claim 14 wherein the second semiconductor material comprises Si_xGe_{1-x}.

18. (Withdrawn) The method of claim 17 wherein the remaining layer has a thickness less than about 15 nm.

19-35. (Cancelled)

36.(New) A field effect transistor (FET) comprising:

a channel core coupled to a substrate and defining a top surface spaced from the substrate and opposed sidewall surfaces between the substrate and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure;

a channel envelope in contact with the opposed sidewall surfaces and the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; ~~and~~

a gate oxide disposed about a surface of the channel envelope that is opposite the channel core; and

a gate coupled to the channel core through the gate oxide, said gate disposed at least partially within the substrate.

37. (New) The FET of claim 36 wherein the said gate is a first gate that extends parallel to one of said opposed sidewall surfaces, the FET further comprising a second gate that extends parallel to the other of said sidewall surfaces.

38. (New) The FET of claim 36 wherein each of said first and second gates are disposed only partially within said substrate.

39. (New) The FET of claim 38 further comprising a third gate disposed parallel to the said top surface and electrically coupling the first and second gates.

40. (New) The FET of claim 39 wherein the third gate is not disposed at least partially within said substrate.

41. (New) The FET of claim 36 wherein the said gate is a first gate that extends parallel to said top surface, the FET further comprising a second gate that extends parallel to said top surface and not disposed at least partially within said substrate.

42. (New) The FET of claim 41 further comprising a third and fourth gate each disposed parallel to said opposed sidewalls and each electrically coupling said first and second gates to one another.

43. (New) A field effect transistor (FET) comprising:

a channel core coupled to a substrate and defining a top surface spaced from the substrate and opposed sidewall surfaces between the substrate and the top surface, wherein the channel core comprises a first semiconductor material defining a first lattice structure;

a channel envelope in contact with the opposed sidewall surfaces and the top surface, wherein the channel envelope comprises a second semiconductor material defining a second lattice structure that differs from the first lattice structure; ~~and~~

a gate oxide disposed about a surface of the channel envelope that is opposite the channel core; and

first and second gates coupled to the channel core through the gate oxide, said first and second gates disposed on opposed sides of said channel core and not directly coupled to one another electrically.

44. (New) The FET of claim 43 wherein said gates are disposed parallel to said top surface.

45. (New) The FET of claim 44 wherein said first gate is at least partially disposed within said substrate.

46. (New) The FET of claim 43 wherein said gates are disposed parallel to said opposed sidewalls.

47. (New) The FET of claim 46 wherein a portion of each of said gates is disposed within said substrate.

48. (New) The FET of claim 43 further comprising a first control coupled to the first gate and a second control for controlling to the second gate, wherein the first and second controls are independent of one another.

49. (New) The FET of claim 48 wherein the first control comprises a first voltage source that applies a variable voltage to the first gate.

50. (New) The FET of claim 49 wherein the second control operates to select between on and off for the second gate, and the first and second controls operate in conjunction with one another.